ADVANCE INFORMATION

AMD

ÉlanSC410™

Single-Chip PC/AT-Compatible Microcontroller

DISTINCTIVE CHARACTERISTICS

- **E86™ family of x86 embedded processors**
  - — Offers improved time-to-market, software migration, and field-proven development tools
- **Highly integrated single-chip CPU with a complete set of common peripherals**
  - — Accelerates time-to-market with simplified hardware
  - — Low-power 0.35 micron process technology
  - — Single chip delivers smallest system form factor
  - — 33-MHz and 66-MHz operating frequencies
  - — No floating point unit
- **Am486® CPU core**
  - — Robust Microsoft® Windows® compatible CPU
  - — 8K write-back cache for enhanced performance
  - — Fully static design with System Management Mode (SMM) for power savings
- **Glueless burst-mode ROM/Flash interface**
  - — Reduces system cost by allowing mask ROM and Flash at the same time with three ROM/ Flash chip selects
- **Glueless DRAM controller**
  - — Allows mixed DRAM types on a per-bank basis to reduce system cost
- **Standard PC/AT system logic (PICs, DMACs, timer, RTC)**
  - — DOS, ROM-DOS, Windows, x86 RTOS, and industry-standard BIOS support
  - — Leverages the benefits of desktop computing environment at embedded price points
- **Local bus and ISA bus interface**
  - — Reduces time-to-market with a wide variety of off-the-shelf companion chips
- **Bidirectional parallel port with EPP mode**
- **16550-compatible UART**
- **IrDA infrared port for wireless communication**
  - — Standard and high-speed
- **Keyboard interface**
  - — Matrix keyboard support with up to 15 rows and 8 columns
  - — SCP-emulation mode for PC/AT and XT keyboard support
- **Comprehensive power management unit**
  - — Seven modes of operation allow fine-tuning of power requirements for maximum battery life
  - — Provides a superset of APM 1.2 features

GENERAL DESCRIPTION

Targeted specifically for embedded systems, the Élan™SC410 microcontroller is a single-chip solution that combines the proven performance of an enhanced Am486 CPU microprocessor with the compatibility of a PC/AT chipset in an advanced 0.35 micron process.

Leveraging the benefits of the x86 desktop computing environment, the ÉlanSC410 microcontroller integrates all of the common logic and I/O functionality associated with an PC/AT computing system into a single device, eliminating the need for multiple peripheral chips.

Fully integrated peripherals include two 8259A-compatible programmable interrupt controllers (PICs), two 8237A-compatible DMA controllers, an 8254-compatible timer, a 16550 UART, an IrDA controller, VL-bus and ISA bus controllers, a real-time clock (RTC), and an EPP parallel port.

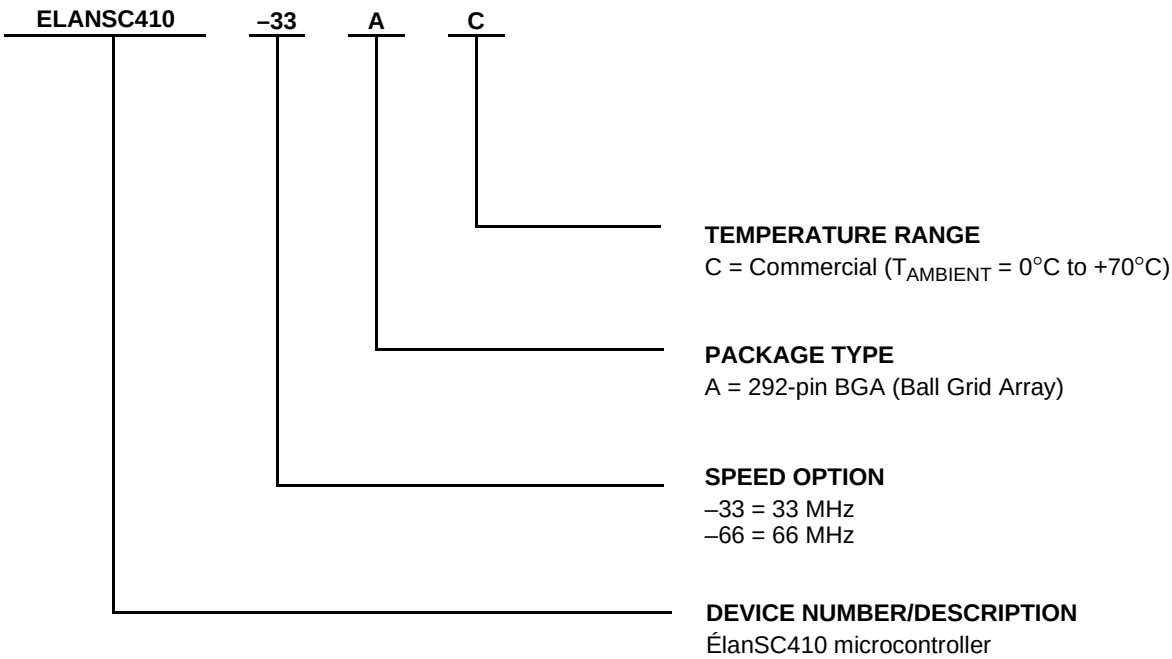
The ÉlanSC410 microcontroller uses the industry-standard 486 microprocessor instruction set. All software written for the x86 architecture family is compatible with the ÉlanSC410 microcontroller.

The ÉlanSC410 microcontroller is a fully static design and includes an advanced power management unit. Operating voltages are 2.7 V–3.3 V with 5-volt-tolerant I/O pads. Orderable in both 33 MHz and 66 MHz peak processor speeds, the product is available in the ultra-small 292 ball grid array (BGA) package.

Publication# **21327** Rev: **A** Amendment
Issue Date: **February 1997**

ORDERING INFORMATION

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

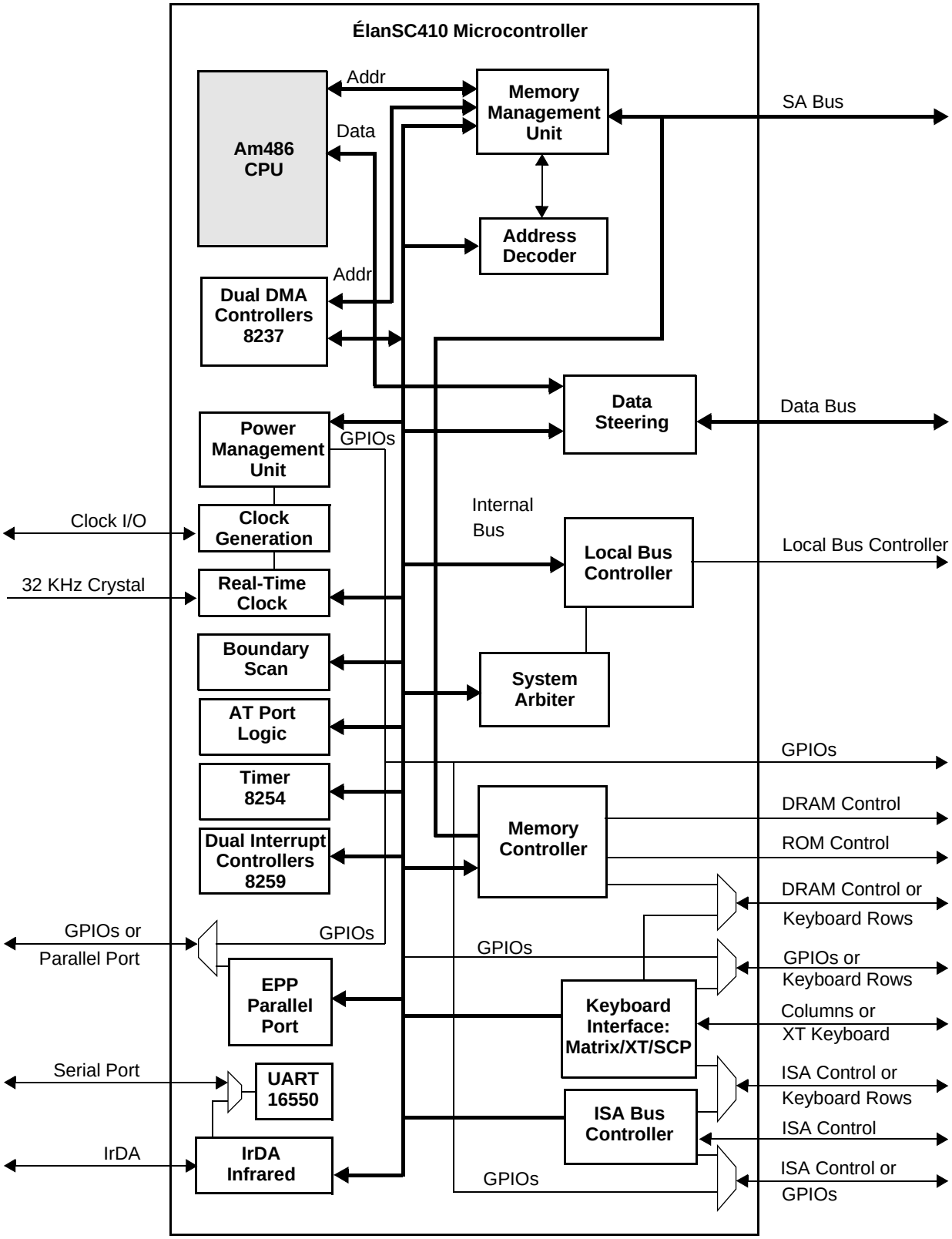


Valid Combinations	
ELANSC410–33	AC
ELANSC410–66	

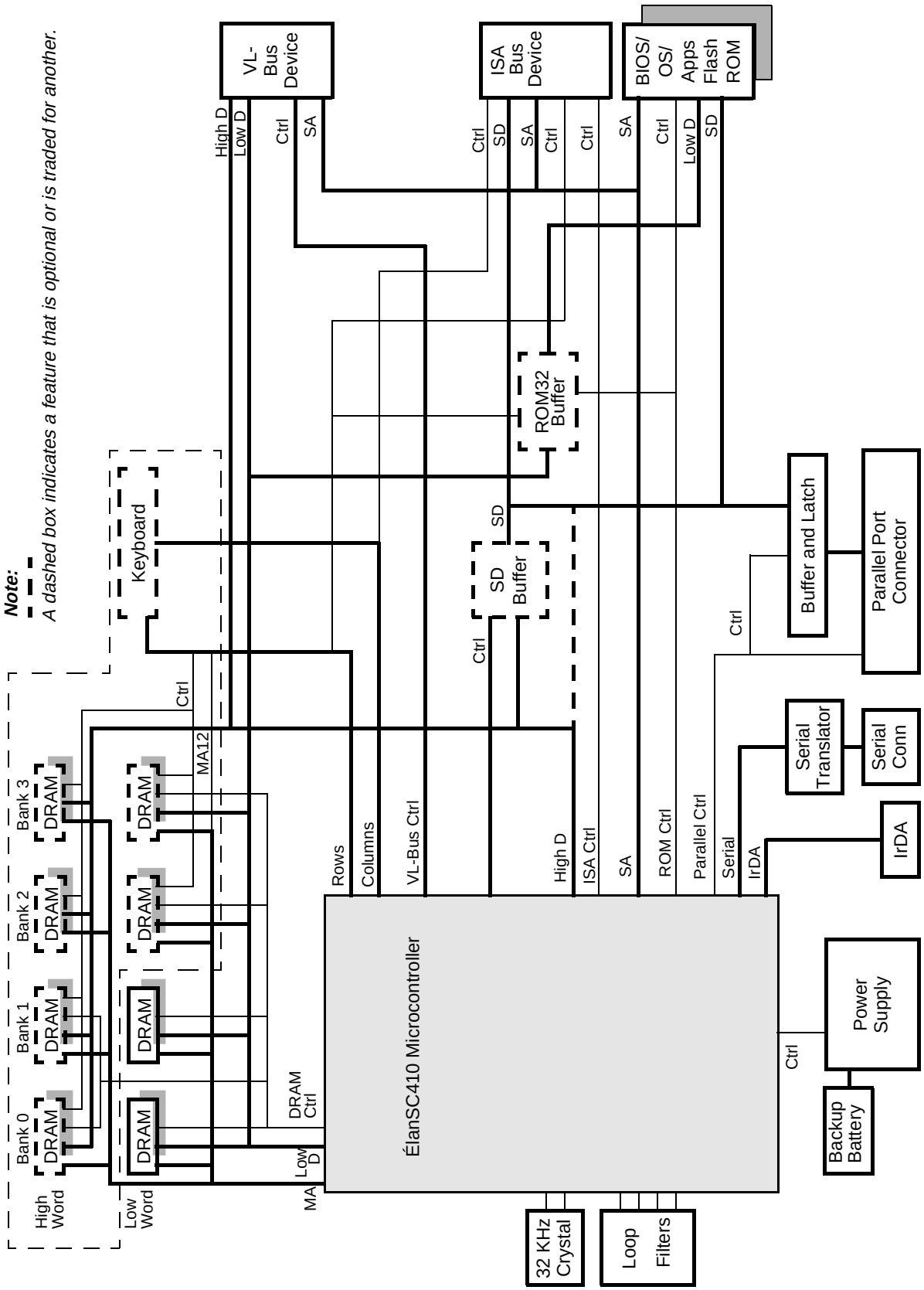
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

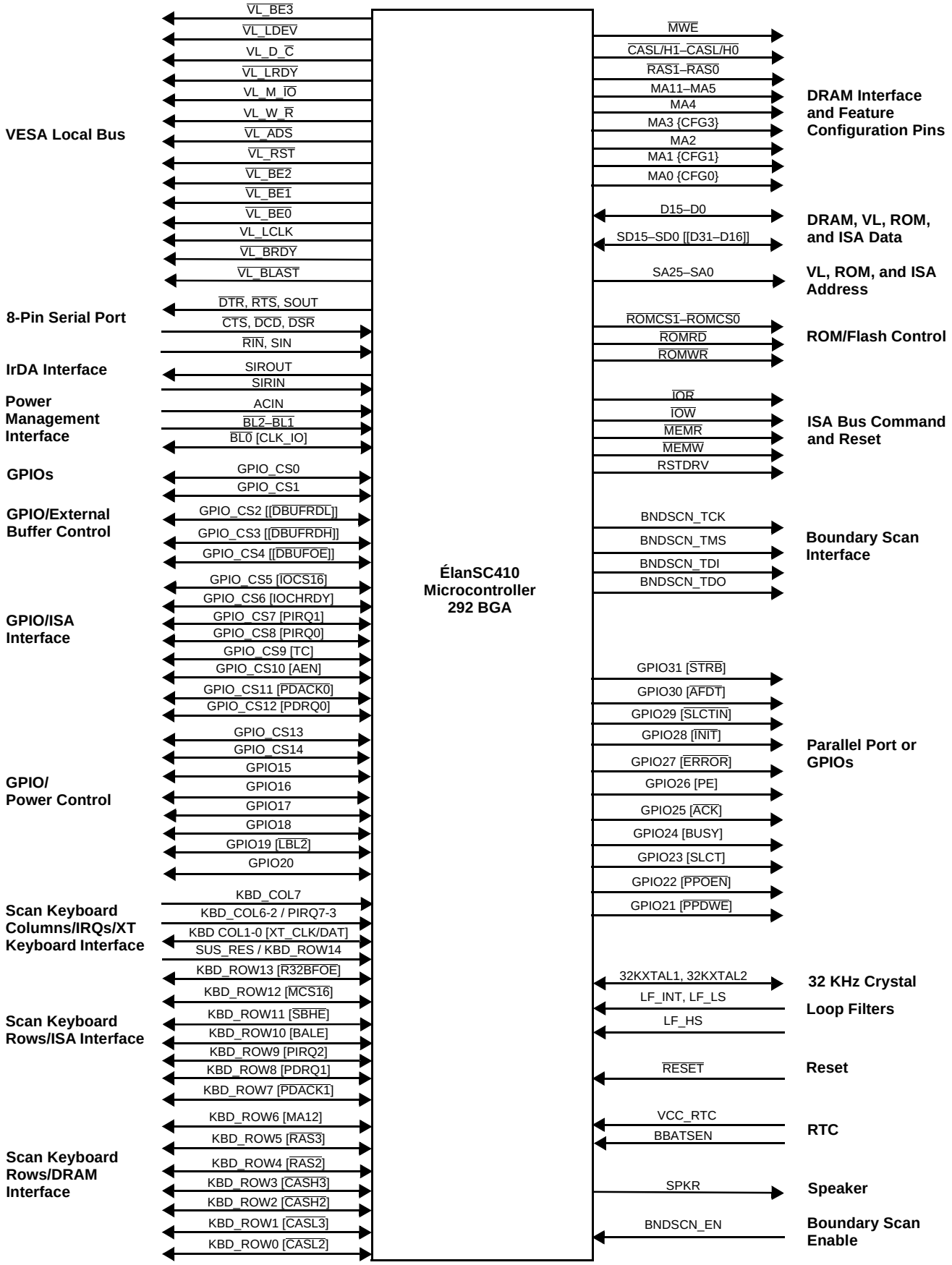
BLOCK DIAGRAM



MAXIMAL SYSTEM DESIGN WITH TRADE-OFFS



LOGIC SYMBOL



Note: *| =Two functions available on the pin at the same time.* { } *= Function during hardware reset.* [ ] *= Alternative function selected by firmware configuration.* [[ ]] *= Alternate function selected by a hardware configuration pin state at power-on reset.*

PIN DESIGNATIONS (Pin Number)—ÉlanSC410 Microcontroller

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
A1	KBD_COL5/PIRQ6	B19	KBD_ROW0 [$\overline{\text{CASL2}}$]	D17	GPIO_CS3 [[$\overline{\text{DBUFRDH}}$]]
A2	KBD_COL2/PIRQ3	B20	$\overline{\text{VL\_RST}}$	D18	$\overline{\text{VL\_W/R}}$
A3	KBD_ROW13 [[$\overline{\text{R32BFOE}}$]]	C1	KBD_ROW11 [$\overline{\text{SBHE}}$]	D19	$\overline{\text{VL\_LRDY}}$
A4	D15	C2	KBD_ROW8 [PDRQ1]	D20	$\overline{\text{VL\_BE3}}$
A5	D12	C3	KBD_COL4/PIRQ5	E1	V_{CC}_BUS
A6	D9	C4	GPIO_CS4 [[$\overline{\text{DBUFOE}}$]]	E2	KBD_COL0 [XT_DATA]
A7	D7	C5	KBD_COL7	E3	KBD_ROW9 [PIRQ2]
A8	V_{CC}_MEM	C6	D13	E4	GND
A9	D4	C7	D10	E17	VCC_VL
A10	D1	C8	D6	E18	VL_D/$\overline{\text{C}}$
A11	$\overline{\text{MWE}}$	C9	D2	E19	VL_LCLK
A12	MA2	C10	MA0 {CFG0}	E20	$\overline{\text{VL\_BE1}}$
A13	V_{CC}_MEM	C11	MA4	F1	SD4 [D20]
A14	MA5	C12	MA7	F2	SD1 [D17]
A15	MA8	C13	MA10	F3	KBD_ROW12 [$\overline{\text{MCS16}}$]
A16	MA11	C14	$\overline{\text{CASL1}}$	F4	GND
A17	$\overline{\text{CASH1}}$	C15	$\overline{\text{RAS0}}$	F17	$\overline{\text{VL\_LDEV}}$
A18	V_{CC}_MEM	C16	KBD_ROW5 [$\overline{\text{RAS3}}$]	F18	$\overline{\text{VL\_BE2}}$
A19	$\overline{\text{VL\_BLAST}}$	C17	KBD_ROW2 [$\overline{\text{CASH2}}$]	F19	$\overline{\text{VL\_BE0}}$
A20	$\overline{\text{VL\_BRDY}}$	C18	GPIO_CS2 [[$\overline{\text{DBUFRDL}}$]]	F20	SA24
B1	V_{CC}_MEM	C19	$\overline{\text{VL\_ADS}}$	G1	SD6 [D22]
B2	KBD_COL6/PIRQ7	C20	VL_M/$\overline{\text{IO}}$	G2	SD3 [D19]
B3	KBD_COL3/PIRQ4	D1	KBD_COL1 [XT_CLK]	G3	SD0 [D16]
B4	V_{CC}_MEM	D2	KBD_ROW10 [BALE]	G4	GND
B5	D14	D3	KBD_ROW7 [$\overline{\text{PDACK1}}$]	G17	VCC_VL
B6	D11	D4	GND	G18	GPIO20
B7	D8	D5	GND	G19	SA22
B8	D5	D6	GND	G20	SA21
B9	D3	D7	GND	H1	V_{CC}_BUS
B10	D0	D8	GND	H2	SD5 [D21]
B11	MA1 {CFG1}	D9	GND	H3	SD2 [D18]
B12	MA3 {CFG3}	D10	GND	H4	GND
B13	MA6	D11	GND	H8	GND
B14	MA9	D12	GND	H9	GND
B15	$\overline{\text{CASL0}}$	D13	$\overline{\text{CASH0}}$	H10	GND
B16	V_{CC}_MEM	D14	$\overline{\text{RAS1}}$	H11	GND
B17	KBD_ROW6 [MA12]	D15	KBD_ROW4 [$\overline{\text{RAS2}}$]	H12	GND
B18	KBD_ROW3 [$\overline{\text{CASH3}}$]	D16	KBD_ROW1 [$\overline{\text{CASL3}}$]	H13	GND

PIN DESIGNATIONS (Pin Number)—ÉlanSC410 Microcontroller (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
H17	SA25	L10	GND	P3	Reserved
H18	SA23	L11	GND	P4	V_{CC}_CPU
H19	SA20	L12	GND	P17	V_{CC}
H20	SA18	L13	GND	P18	V_{CC}_SYS
J1	SD10 [D26]	L17	V_{CC}	P19	SA1
J2	SD7 [D23]	L18	SA10	P20	SA4
J3	V_{CC}_BUS	L19	SA9	R1	[[BDNSCN_TDI]]
J4	GND	L20	SA11	R2	Reserved
J8	GND	M1	V_{CC}_BUS	R3	Reserved
J9	GND	M2	[[BDNSCN_TDO]]	R4	V_{CC}_CPU
J10	GND	M3	Reserved	R17	GND
J11	GND	M4	V_{CC}_CPU	R18	$\overline{\text{ROMCS0}}$
J12	GND	M8	GND	R19	$\overline{\text{IOW}}$
J13	GND	M9	GND	R20	SA2
J17	V_{CC}_SYS	M10	GND	T1	VCC_PP
J18	SA19	M11	GND	T2	Reserved
J19	SA17	M12	GND	T3	GPIO22 [$\overline{\text{PPOEN}}$]
J20	SA14	M13	GND	T4	V_{CC}_CPU
K1	SD11 [D27]	M17	V_{CC}	T17	GND
K2	SD9 [D25]	M18	SA7	T18	$\overline{\text{MEMW}}$
K3	SD8 [D24]	M19	V_{CC}_SYS	T19	$\overline{\text{ROMCS1}}$
K4	V_{CC}_CPU	M20	SA8	T20	SA0
K8	GND	N1	SD14 [D30]	U1	Reserved
K9	GND	N2	Reserved	U2	GPIO25 [$\overline{\text{ACK}}$]
K10	GND	N3	[[BDNSCN_TMS]]	U3	GPIO24 [BUSY]
K11	GND	N4	V_{CC}_CPU	U4	GPIO23 [SLCT]
K12	GND	N8	GND	U5	GND
K13	GND	N9	GND	U6	GND
K17	SA16	N10	GND	U7	GND
K18	SA15	N11	GND	U8	GND
K19	SA13	N12	GND	U9	GND
K20	SA12	N13	GND	U10	GND
L1	SD12 [D28]	N17	V_{CC}	U11	GND
L2	SD13 [D29]	N18	SA3	U12	GND
L3	SD15 [D31]	N19	SA5	U13	GND
L4	V_{CC}_CPU	N20	SA6	U14	GND
L8	GND	P1	Reserved	U15	GND
L9	GND	P2	[[BDNSCN_TCK]]	U16	GND

PIN DESIGNATIONS (Pin Number)—ÉlanSC410 Microcontroller (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
U17	GND	V19	GPIO_CS0	Y1	VCC_PP
U18	V_{CC}_SYS	V20	$\overline{\text{ROMRD}}$	Y2	GPIO28 [$\overline{\text{INIT}}$]
U19	$\overline{\text{ROMWR}}$	W1	GPIO30 [$\overline{\text{AFDT}}$]	Y3	LF_INT
U20	$\overline{\text{IOR}}$	W2	GPIO26 [PE]	Y4	32KXTAL2
V1	Reserved	W3	GPIO29 [$\overline{\text{SLCTIN}}$]	Y5	GND_ANALOG
V2	GPIO31 [$\overline{\text{STRB}}$]	W4	LF_LS	Y6	32KXTAL1
V3	GPIO21 [$\overline{\text{PPDWE}}$]	W5	Reserved	Y7	$\overline{\text{RESET}}$
V4	GPIO27 [$\overline{\text{ERROR}}$]	W6	V_{CC}_A	Y8	$\overline{\text{DTR}}$
V5	LF_HS	W7	V_{CC}_RTC	Y9	SIRIN
V6	BBATSEN	W8	$\overline{\text{RTS}}$	Y10	SOUT
V7	SPKR	W9	V_{CC}_SER	Y11	BNDSCN_EN
V8	SIROUT	W10	$\overline{\text{DSR}}$	Y12	SUS_RES/KBD_ROW14
V9	$\overline{\text{DCD}}$	W11	SIN	Y13	$\overline{\text{BL1}}$
V10	$\overline{\text{CTS}}$	W12	ACIN	Y14	GPIO18
V11	$\overline{\text{RIN}}$	W13	$\overline{\text{BL2}}$	Y15	GPIO15
V12	RSTDRV	W14	$\overline{\text{BL0}}$ [CLK_IO]	Y16	V_{CC}_SYS
V13	V_{CC}_SYS	W15	GPIO17	Y17	GPIO_CS12 [PDRQ0]
V14	GPIO19 [LBL2]	W16	GPIO_CS14	Y18	GPIO_CS9 [TC]
V15	GPIO16	W17	GPIO_CS11 [$\overline{\text{PDACK0}}$]	Y19	GPIO_CS7 [PIRQ1]
V16	GPIO_CS13	W18	GPIO_CS8 [PIRQ0]	Y20	GPIO_CS1
V17	GPIO_CS10 [AEN]	W19	GPIO_CS5 [$\overline{\text{IOCS16}}$]		
V18	GPIO_CS6 [IOCHRDY]	W20	$\overline{\text{MEMR}}$		

PIN DESIGNATIONS (Pin Name)—ÉlanSC410 Microcontroller

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
ACIN	W12	**D10**	C7	**GND**	E4
[$\overline{\text{ACK}}$] GPIO25	U2	**D11**	B6	**GND**	F4
[AEN] GPIO_CS10	V17	**D12**	A5	**GND**	G4
[$\overline{\text{AFDT}}$] GPIO30	W1	**D13**	C6	**GND**	H4
[BALE] KBD_ROW10	D2	**D14**	B5	**GND**	H8
BBATSEN	V6	**D15**	A4	**GND**	H9
BNDSCN_EN	Y11	**[D16] SD0**	G3	**GND**	H10
[[BDNSCN_TCK]]	P2	**[D17] SD1**	F2	**GND**	H11
[[BDNSCN_TDI]]	R1	**[D18] SD2**	H3	**GND**	H12
[[BNDSCN_TDO]]	M2	**[D19] SD3**	G2	**GND**	H13
[[BDNSCN_TMS]]	N3	**[D20] SD4**	F1	**GND**	J4
$\overline{\text{BL0}}$ [CLK_IO]	W14	**[D21] SD5**	H2	**GND**	J8
$\overline{\text{BL1}}$	Y13	**[D22] SD6**	G1	**GND**	J9
$\overline{\text{BL2}}$	W13	**[D23] SD7**	J2	**GND**	J10
[BUSY] GPIO24	U3	**[D24] SD8**	K3	**GND**	J11
$\overline{\text{CASH0}}$	D13	**[D25] SD9**	K2	**GND**	J12
$\overline{\text{CASH1}}$	A17	**[D26] SD10**	J1	**GND**	J13
[$\overline{\text{CASH2}}$] KBD_ROW2	C17	**[D27] SD11**	K1	**GND**	K8
[$\overline{\text{CASH3}}$] KBD_ROW3	B18	**[D28] SD12**	L1	**GND**	K9
$\overline{\text{CASL0}}$	B15	**[D29] SD13**	L2	**GND**	K10
$\overline{\text{CASL1}}$	C14	**[D30] SD14**	N1	**GND**	K11
[$\overline{\text{CASL2}}$] KBD_ROW0	B19	**[D31] SD15**	L3	**GND**	K12
[$\overline{\text{CASL3}}$] KBD_ROW1	D16	**[[$\overline{\text{DBUFOE}}$]] GPIO_CS4**	C4	**GND**	K13
{CFG0} MA0	C10	**[[$\overline{\text{DBUFRDH}}$]] GPIO_CS3**	D17	**GND**	L8
{CFG1} MA1	B11	**[[$\overline{\text{DBUFRDL}}$]] GPIO_CS2**	C18	**GND**	L9
{CFG3} MA3	B12	**$\overline{\text{DCD}}$**	V9	**GND**	L10
[CLK_IO] $\overline{\text{BL0}}$	W14	**$\overline{\text{DSR}}$**	W10	**GND**	L11
$\overline{\text{CTS}}$	V10	**$\overline{\text{DTR}}$**	Y8	**GND**	L12
D0	B10	**[$\overline{\text{ERROR}}$] GPIO27**	V4	**GND**	L13
D1	A10	**GND**	D4	**GND**	M8
D2	C9	**GND**	D5	**GND**	M9
D3	B9	**GND**	D6	**GND**	M10
D4	A9	**GND**	D7	**GND**	M11
D5	B8	**GND**	D8	**GND**	M12
D6	C8	**GND**	D9	**GND**	M13
D7	A7	**GND**	D10	**GND**	N8
D8	B7	**GND**	D11	**GND**	N9
D9	A6	**GND**	D12	**GND**	N10

PIN DESIGNATIONS (Pin Name)—ÉlanSC410 Microcontroller (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
GND	N11	**GPIO19 [LBL2]**	V14	**KBD_ROW10 [BALE]**	D2
GND	N12	**GPIO20**	G18	**KBD_ROW11 [SBHE]**	C1
GND	N13	**GPIO21 [$\overline{\text{PPDWE}}$]**	V3	**KBD_ROW12 [$\overline{\text{MCS16}}$]**	F3
GND	R17	**GPIO22 [$\overline{\text{PPOEN}}$]**	T3	**KBD_ROW13 [[$\overline{\text{R32BFOE}}$]]**	A3
GND	T17	**GPIO23 [SLCT]**	U4	**KBD_ROW14 / SUS_RES**	Y12
GND	U5	**GPIO24 [BUSY]**	U3	**[LBL2] GPIO19**	V14
GND	U6	**GPIO25 [$\overline{\text{ACK}}$]**	U2	**LF_HS**	V5
GND	U7	**GPIO26 [PE]**	W2	**LF_INT**	Y3
GND	U8	**GPIO27 [$\overline{\text{ERROR}}$]**	V4	**LF_LS**	W4
GND	U9	**GPIO28 [$\overline{\text{INIT}}$]**	Y2	**MA0 {CFG0}**	C10
GND	U10	**GPIO29 [$\overline{\text{SLCTIN}}$]**	W3	**MA1 {CFG1}**	B11
GND	U11	**GPIO30 [$\overline{\text{AFDT}}$]**	W1	**MA2**	A12
GND	U12	**GPIO31 [$\overline{\text{STRB}}$]**	V2	**MA3 {CFG3}**	B12
GND	U13	**[$\overline{\text{INIT}}$] GPIO28**	Y2	**MA4**	C11
GND	U14	**[IOCHRDY] GPIO_CS6**	V18	**MA5**	A14
GND	U15	**[$\overline{\text{IOCS16}}$] GPIO_CS5**	W19	**MA6**	B13
GND	U16	**$\overline{\text{IOR}}$**	U20	**MA7**	C12
GND	U17	**$\overline{\text{IOW}}$**	R19	**MA8**	A15
GND_ANALOG	Y5	**32KXTAL1**	Y6	**MA9**	B14
GPIO_CS0	V19	**32KXTAL2**	Y4	**MA10**	C13
GPIO_CS1	Y20	**KBD_COL0 [$\overline{\text{XT_DATA}}$]**	E2	**MA11**	A16
GPIO_CS2 [[$\overline{\text{DBUFRDL}}$]]	C18	**KBD_COL1 [XT_CLK]**	D1	**[MA12] KBD_ROW6**	B17
GPIO_CS3 [[$\overline{\text{DBUFRDH}}$]]	D17	**KBD_COL2/PIRQ3**	A2	**[$\overline{\text{MCS16}}$] KBD_ROW12**	F3
GPIO_CS4 [[$\overline{\text{DBUFOE}}$]]	C4	**KBD_COL3/PIRQ4**	B3	**$\overline{\text{MEMR}}$**	W20
GPIO_CS5 [$\overline{\text{IOCS16}}$]	W19	**KBD_COL4/PIRQ5**	C3	**$\overline{\text{MEMW}}$**	T18
GPIO_CS6 [IOCHRDY]	V18	**KBD_COL5/PIRQ6**	A1	**$\overline{\text{MWE}}$**	A11
GPIO_CS7 [PIRQ1]	Y19	**KBD_COL6/PIRQ7**	B2	**[$\overline{\text{PDACK0}}$] GPIO_CS11**	W17
GPIO_CS8 [PIRQ0]	W18	**KBD_COL7**	C5	**[$\overline{\text{PDACK1}}$] KBD_ROW7**	D3
GPIO_CS9 [TC]	Y18	**KBD_ROW0 [$\overline{\text{CASL2}}$]**	B19	**[PDRQ0] GPIO_CS12**	Y17
GPIO_CS10 [AEN]	V17	**KBD_ROW1 [$\overline{\text{CASL3}}$]**	D16	**[PDRQ1] KBD_ROW8**	C2
GPIO_CS11 [$\overline{\text{PDACK0}}$]	W17	**KBD_ROW2 [$\overline{\text{CASH2}}$]**	C17	**[PE] GPIO26**	W2
GPIO_CS12 [PDRQ0]	Y17	**KBD_ROW3 [$\overline{\text{CASH3}}$]**	B18	**[PIRQ0] GPIO_CS8**	W18
GPIO_CS13	V16	**KBD_ROW4 [$\overline{\text{RAS2}}$]**	D15	**[PIRQ1] GPIO_CS7**	Y19
GPIO_CS14	W16	**KBD_ROW5 [$\overline{\text{RAS3}}$]**	C16	**[PIRQ2] KBD_ROW9**	E3
GPIO15	Y15	**KBD_ROW6 [MA12]**	B17	**PIRQ3/KBD_COL2**	A2
GPIO16	V15	**KBD_ROW7 [$\overline{\text{PDACK1}}$]**	D3	**PIRQ4/KBD_COL3**	B3
GPIO17	W15	**KBD_ROW8 [PDRQ1]**	C2	**PIRQ5/KBD_COL4**	C3
GPIO18	Y14	**KBD_ROW9 [PIRQ2]**	E3	**PIRQ6/KBD_COL5**	A1

PIN DESIGNATIONS (Pin Name)—ÉlanSC410 Microcontroller (Continued)

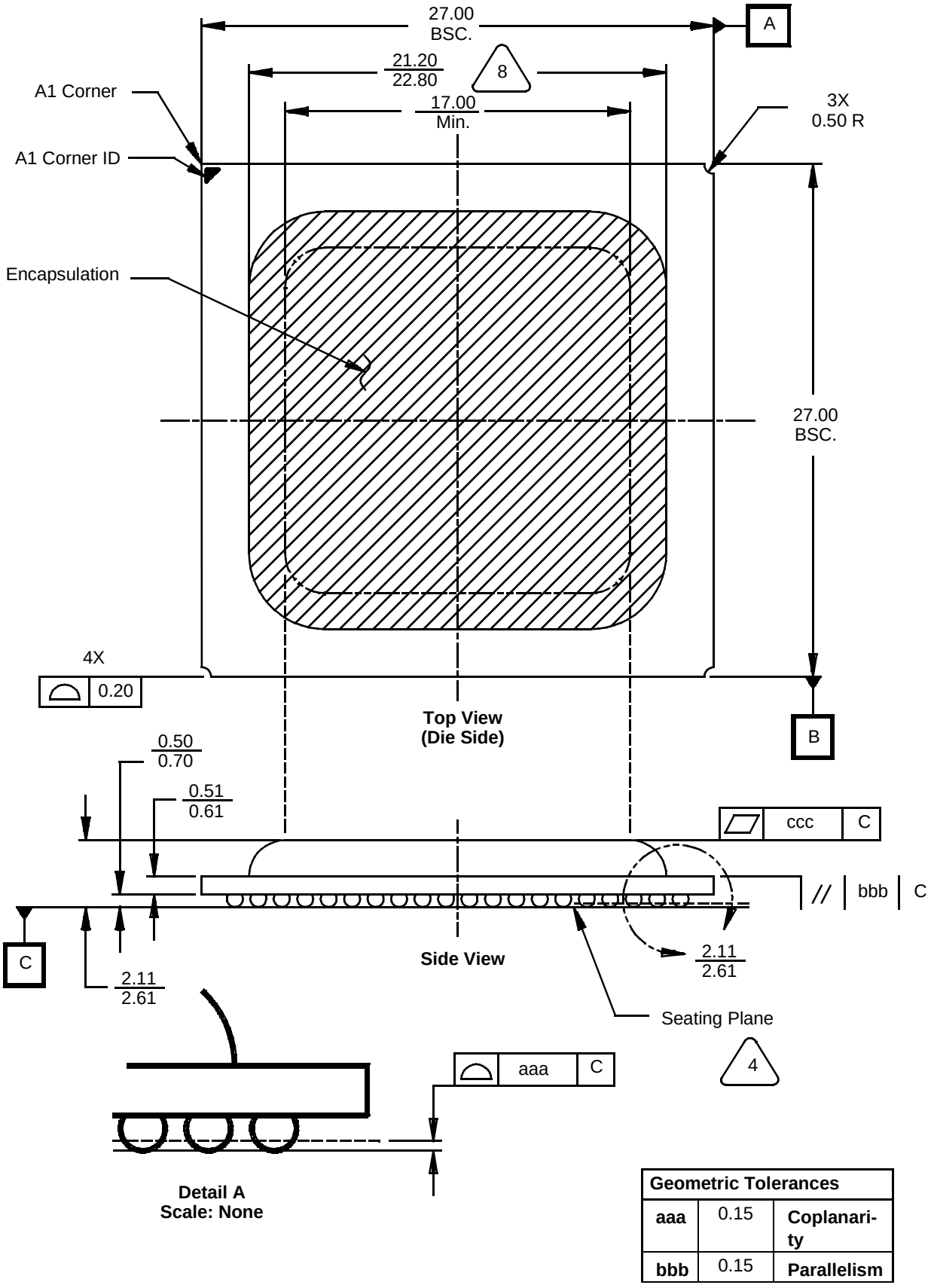
Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
PIRQ7/KBD_COL6	B2	**SA12**	K20	**[$\overline{\text{STRB}}$] GPIO31**	V2
[$\overline{\text{PPDWE}}$] GPIO21	V3	**SA13**	K19	**SUS_RES/KBD_ROW14**	Y12
[$\overline{\text{PPOEN}}$] GPIO22	T3	**SA14**	J20	**[TC] GPIO_CS9**	Y18
[[$\overline{\text{R32BFOE}}$]] KBD_ROW13	A3	**SA15**	K18	**VCC**	L17
$\overline{\text{RAS0}}$	C15	**SA16**	K17	**VCC**	M17
$\overline{\text{RAS1}}$	D14	**SA17**	J19	**VCC**	N17
[$\overline{\text{RAS2}}$] KBD_ROW4	D15	**SA18**	H20	**VCC**	P17
[$\overline{\text{RAS3}}$] KBD_ROW5	C16	**SA19**	J18	**VCC_A**	W6
Reserved	M3	**SA20**	H19	**VCC_BUS**	E1
Reserved	N2	**SA21**	G20	**VCC_BUS**	H1
Reserved	P1	**SA22**	G19	**VCC_BUS**	J3
Reserved	P3	**SA23**	H18	**VCC_BUS**	M1
Reserved	R2	**SA24**	F20	**VCC_CPU**	K4
Reserved	R3	**SA25**	H17	**VCC_CPU**	L4
Reserved	T2	**[$\overline{\text{SBHE}}$] KBD_ROW11**	C1	**VCC_CPU**	M4
Reserved	U1	**SD0 [D16]**	G3	**VCC_CPU**	N4
Reserved	V1	**SD1 [D17]**	F2	**VCC_CPU**	P4
Reserved	W5	**SD2 [D18]**	H3	**VCC_CPU**	R4
$\overline{\text{RESET}}$	Y7	**SD3 [D19]**	G2	**VCC_CPU**	T4
$\overline{\text{RIN}}$	V11	**SD4 [D20]**	F1	**VCC_MEM**	A8
$\overline{\text{ROMCS0}}$	R18	**SD5 [D21]**	H2	**VCC_MEM**	A13
$\overline{\text{ROMCS1}}$	T19	**SD6 [D22]**	G1	**VCC_MEM**	A18
$\overline{\text{ROMRD}}$	V20	**SD7 [D23]**	J2	**VCC_MEM**	B1
$\overline{\text{ROMWR}}$	U19	**SD8 [D24]**	K3	**VCC_MEM**	B4
RSTDRV	V12	**SD9 [D25]**	K2	**VCC_MEM**	B16
$\overline{\text{RTS}}$	W8	**SD10 [D26]**	J1	**VCC_PP**	T1
SA0	T20	**SD11 [D27]**	K1	**VCC_PP**	Y1
SA1	P19	**SD12 [D28]**	L1	**VCC_RTC**	W7
SA2	R20	**SD13 [D29]**	L2	**VCC_SER**	W9
SA3	N18	**SD14 [D30]**	N1	**VCC_SYS**	J17
SA4	P20	**SD15 [D31]**	L3	**VCC_SYS**	M19
SA5	N19	**SIN**	W11	**VCC_SYS**	P18
SA6	N20	**SIRIN**	Y9	**VCC_SYS**	U18
SA7	M18	**SIROUT**	V8	**VCC_SYS**	V13
SA8	M20	**[SLCT] GPIO23**	U4	**VCC_SYS**	Y16
SA9	L19	**[$\overline{\text{SLCTIN}}$] GPIO29**	W3	**VCC-VL**	E17
SA10	L18	**SOUT**	Y10	**VCC_VL**	G17
SA11	L20	**SPKR**	V7	**$\overline{\text{VL\_ADS}}$**	C19

PIN DESIGNATIONS (Pin Name)—ÉlanSC410 Microcontroller (Continued)

Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.
VL_BE0	F19	**VL_BRDY**	A20	**VL_M/IO**	C20
VL_BE1	E20	**VL_D/C**	E18	**VL_RST**	B20
VL_BE2	F18	**VL_LCLK**	E19	**VL_W/R**	D18
VL_BE3	D20	**VL_LDEV**	F17	**[XT_CLK] KBD_COL1**	D1
VL_BLAST	A19	**VL_LRDY**	D19	**[XT_DATA] KBD_COL0**	E2

PHYSICAL DIMENSIONS

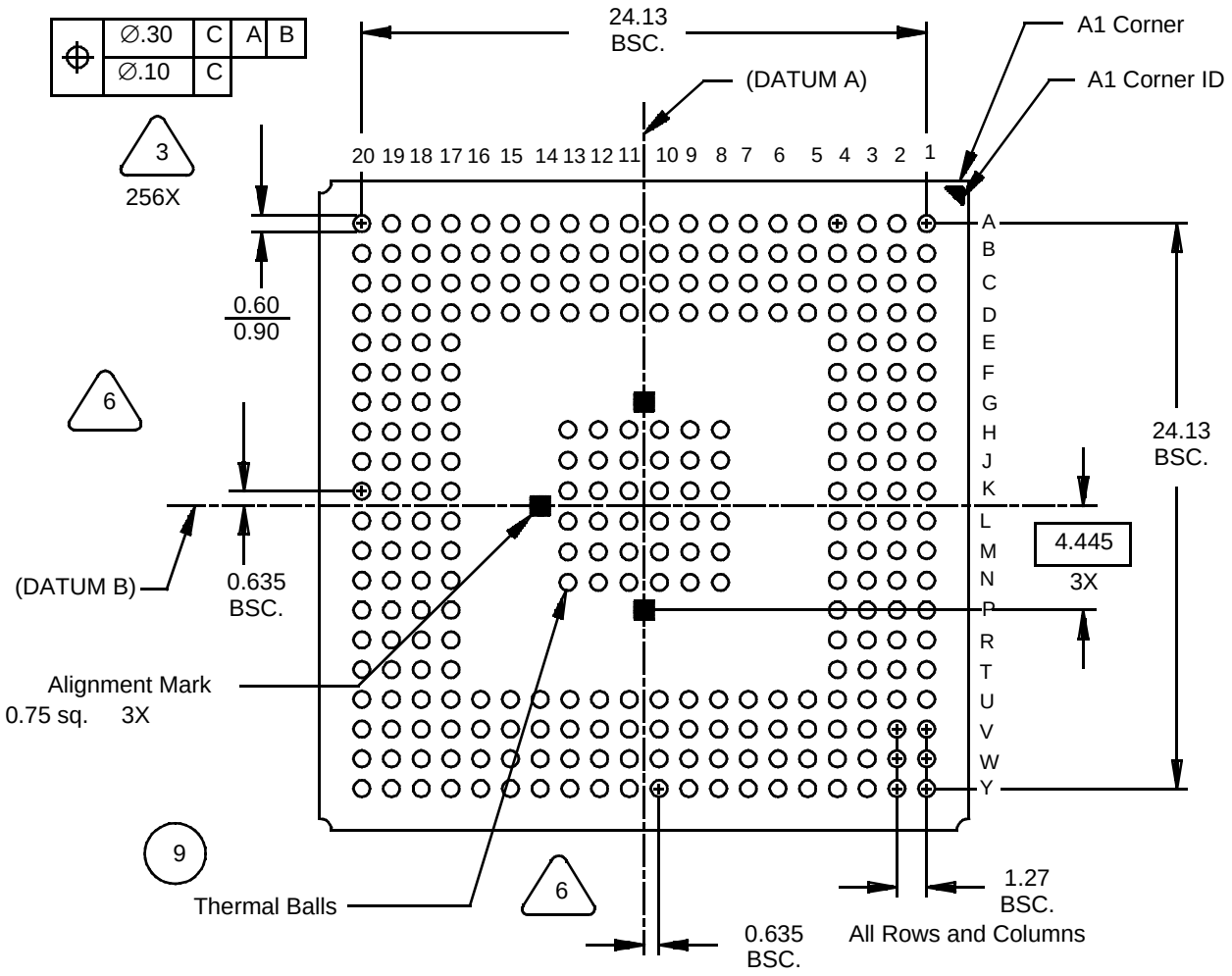
BGA 292—Plastic Ball Grid Array



Geometric Tolerances		
aaa	0.15	**Coplanarity**
bbb	0.15	**Parallelism**

PHYSICAL DIMENSIONS (CONTINUED)

BGA 292



Bottom View

Notes:

1. *All dimensions and tolerances conform to ASME Y14.5M-1994.*
2. *All dimensions are in millimeters.*
3. *Dimension b is measured at the maximum solder ball diameter on a plane parallel to DATUM C.*
4. *DATUM C and seating plane are defined by the spherical crowns of the solder balls.*
5. *Number of peripheral rows or columns*
6. *S is measured with respect to DATUMS A and B and defines the position of the solder balls nearest the package centerlines.*
7. *Conforms to JEP–95, MO–151, Issue B, Variation BAL–2.*
8. *Corners of encapsulation area need not be square. (Unspecified radius)*
9. *Package has a 6x6 matrix of thermal balls at the package center. The balls are connected to ground.*
10. *Not to scale. For reference only.*